Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Please amend the claims as specified.

Claims 1-9 (cancelled)

Claim 10 (new): A sequencer for applying a first signal and a second signal to a circuit based on the state of the first signal in comparison to the second signal comprising:

a comparison circuit for generating a third signal based upon a comparison of a fourth signal derived from the second signal to a fifth signal derived from the first signal;

a bias generation circuit for generating a plurality of gate control signals from the first signal and the second signal; and

a back gate bias application circuit responsive to the plurality of gate control signals regulating application of the first signal and the second signal to the circuit.

Claim 11 (new): The sequencer of claim 10, wherein the comparison circuit further comprises:

a first divider coupled to the first signal for producing a first reference level;

a second divider coupled to the second signal for producing a second reference level; and

a comparator having a first comparator input coupled to the first reference level and a second comparator input coupled to the second reference level for comparing the first reference level to the second reference level.

Claim 12 (new): The sequencer of claim 11, wherein the first divider is a resistive divider.

Claim 13 (new): The sequencer of claim 11, wherein the second divider comprises:

a current source having an input coupled to the second signal;

a diode chain, with the input of the diode chain coupled to the second comparator input and coupled to the output of the current source for establishing the second reference level in response to the current source.

Claim 14 (new): The sequencer of claim 13, wherein the diode chain comprises a plurality of series coupled diodes providing a current path for the current source and providing a desired voltage drop as the second reference level due to a current flow through the plurality of diodes.

Claim 15 (new): The sequencer of claim 10, wherein the bias generation circuit comprises:

a first inverter having an input coupled to the comparator output;

a second inverter, including a voltage dropping transistor, having an input coupled to the comparator output and an output coupled to a first output gate control signal; and

a third inverter with diode level shifters having an input coupled to a first inverter output and an output coupled to a second output gate control signal and the second inverter input.

Claim 16 (new): The sequencer of claim 15, wherein the second inverter comprises:

a PMOS transistor with a source terminal coupled to a high voltage, a back gate terminal coupled to the source terminal, and a gate terminal coupled to the second output gate control signal;

a first NMOS transistor having a drain terminal coupled to a drain terminal of the PMOS transistor, a back gate terminal coupled to a ground, and a gate terminal coupled to the comparator output; and

a second NMOS transistor having a drain terminal coupled to a source terminal of the first NMOS transistor, a back gate terminal coupled to the ground, and a gate terminal coupled to the comparator output.

Claim 17 (new): The sequencer of claim 15, wherein the third inverter comprises:

a PMOS transistor with a source terminal coupled to a low voltage, a back gate terminal coupled to the source terminal, and a gate terminal coupled to the first inverter output;

a first NMOS transistor having a drain terminal coupled to a drain terminal of the PMOS transistor, a back gate terminal coupled to a ground, and a gate terminal coupled to the first NMOS transistor drain terminal;

a current source coupled from the PMOS transistor source terminal to the PMOS transistor drain terminal;

a second NMOS transistor having a drain terminal coupled to a first NMOS transistor source terminal, a back gate terminal coupled to the ground, and a gate terminal coupled to the first inverter output; and

a third NMOS transistor having a drain terminal coupled to a second NMOS transistor source terminal, a back gate terminal coupled to the ground, a gate terminal coupled to the second NMOS transistor drain terminal, and a source terminal coupled to the ground.

Claim 18 (new): The sequencer of claim 10, wherein the back gate bias application circuit comprises:

a first transistor having a source terminal coupled to the first signal and a gate terminal coupled to the first gate control signal; and

a second transistor having a source terminal coupled to the second signal, a drain terminal coupled to a drain terminal of the first transistor, a back gate coupled to a back gate of the first transistor and the circuit, and a gate terminal coupled to the second gate control signal.

Claim 19 (new): The sequencer of claim 10, further comprising a substrate upon which the sequencer is disposed.

Claim 20 (new): A protection circuit for applying differing voltages to integrated circuits in a controlled manner to a plurality of circuits including a first circuit powered by a first voltage and a second circuit powered by a second voltage, the second voltage being less than the first voltage, comprising:

a back gate, wherein the second circuit includes the back gate;

a back gate bias application circuit coupled to the first voltage, the second voltage, and the back gate providing a selective application of the first voltage and the second voltage to the back gate; and

a controller circuit responsive to the first voltage and the second voltage to control the selective application of the first voltage and the second voltage to the back gate through control of the back gate bias application circuit.

Claim 21 (new): The protection circuit of claim 20, further comprising:

a modified I/O cell having a plurality of transistors having a plurality of corresponding back gates for each of the plurality of transistors, wherein the second circuit includes the modified I/O cell.

Claim 22 (new): The protection circuit of claim 21, wherein each of the plurality of transistors of the modified I/O cell has a source terminal coupled to the second voltage and a drain terminal available as an I/O connection.

Claim 23 (new): The protection circuit of claim 20, wherein the back gate bias application circuit comprises a switch for applying the first voltage and the second voltage to the back gate as controlled by the controller circuit.

Claim 24 (new): The protection circuit of claim 23, wherein the switch includes transistors to couple the first voltage and the second voltage to the back gate.

Claim 25 (new): The protection circuit of claim 20, wherein the controller circuit includes a first controller circuit output and a second controller circuit output.

Claim 26 (new): The protection circuit of claim 25, wherein:

the back gate bias application circuit includes a first transistor and a second transistor common drain coupled to the back gate, the first transistor having a source coupled to the first voltage and a gate coupled to the controller circuit and the second transistor having a second source coupled to the second voltage and a gate coupled to the controller circuit,

whereby first and second controller circuit output signals applied to the first and second gates control the application of the first voltage and the second voltage to the back gate such that the second circuit is protected.

Claim 27 (new): The protection circuit of claim 20, further comprising:

a high supply connection coupling the first voltage to the second circuit, wherein the second circuit includes the high supply connection,

wherein the back gate is coupled to the first voltage via the high supply connection.

Claim 28 (new): A method of controlling the application of a first signal and a second signal to a circuit based upon a state of the first signal relative to the second signal as processed by a controller circuit and a back gate bias application circuit comprising:

applying the second signal to the circuit;

sensing the state of the first signal;

producing a first reference signal based on the sensed state of the first signal;

sensing a state of the second signal;

producing a second reference signal based on the sensed state of the second signal;

comparing the first reference signal to the second reference signal; and

applying the first signal to the circuit when the first reference signal exceeds the second reference signal in level.

Claim 29 (new): The method of claim 28, wherein:

the first signal is a first power supply voltage;

the first reference signal is a first voltage;

the second signal is a second power supply voltage; and

the second reference signal is a second voltage.